

What is claimed is:

1. A semiconductor structure, comprising:
a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom; and
a dielectric cap on a top of the sidewalls.
2. The semiconductor structure of claim 1, wherein the conductive container structure has a cylindrical shape.
3. The semiconductor structure of claim 1, wherein the closed bottom and sidewalls comprise at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
4. The semiconductor structure of claim 3, wherein the at least one silicon material is conductively doped.
5. The semiconductor structure of claim 1, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.
6. A semiconductor structure, comprising:
a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the closed bottom and sidewalls comprise at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
and

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

7. The semiconductor structure of claim 6, wherein the dielectric cap is annealed.

8. A semiconductor structure, comprising:
a conductive container structure having sidewalls, wherein the conductive container structure comprises conductively-doped hemispherical grain polysilicon; and
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride.

9. The semiconductor structure of claim 8, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.

10. A method of forming a semiconductor structure, comprising:
forming an insulating layer on a substrate;
forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
forming a conductive layer on the insulating layer and the exposed portion of the substrate;
forming a fill layer on the conductive layer, wherein the fill layer fills the opening;
removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a

closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer; removing the fill layer to expose an inside of the container structure; and removing at least a portion of the insulating layer to expose an outside of the container structure.

11. The method of claim 10, wherein the processing proceeds in the order presented.
12. The method of claim 10, wherein removing at least a portion of the insulating layer to expose an outside of the container structure occurs subsequent to forming a dielectric cap on a top of the sidewalls of the conductive layer.
13. The method of claim 10, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:
 - forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and
 - removing the dielectric layer from the insulating layer and the fill layer.
14. The method of claim 13, wherein removing the dielectric layer from the insulating layer and the fill layer further comprises removing the dielectric layer from the insulating layer and the fill layer using an anisotropic etch.
15. The method of claim 10, wherein forming an insulating layer on a substrate further comprises forming a layer of borophosphosilicate glass on the substrate.
16. The method of claim 10, wherein forming a conductive layer on the insulating layer and the exposed portion of the substrate further comprises forming a layer

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of conductively-doped hemispherical grain polysilicon on the insulating layer and the exposed portion of the substrate.

17. The method of claim 10, wherein forming a fill layer on the conductive layer further comprises forming a layer of photoresist on the conductive layer.
18. The method of claim 10, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises forming a cap of silicon oxynitride on a top of the sidewalls of the conductive layer.
19. The method of claim 10, further comprising:
annealing the dielectric cap.
20. A method of forming a semiconductor structure, comprising:
forming an insulating layer on a substrate, wherein the insulating layer comprises at least one insulating material selected from the group consisting of oxides, nitrides and borophosphosilicate glass;
forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
forming a conductive layer on the insulating layer and the exposed portion of the substrate, wherein the conductive layer comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
forming a fill layer on the conductive layer, wherein the fill layer fills the opening, further wherein the fill layer comprises a filler material selected from the group consisting of photoresists and high etch-rate oxides;
removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls

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comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

removing the fill layer to expose an inside of the container structure; and removing at least a portion of the insulating layer to expose an outside of the container structure.

21. The method of claim 20, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:
 - forming a layer of the at least one dielectric material on the insulating layer, the conductive layer and the fill layer; and
 - removing the layer of the at least one dielectric material from the insulating layer and the fill layer.
22. The method of claim 20, further comprising:
 - annealing the dielectric cap.
23. A method of forming a semiconductor structure, comprising:
 - forming an insulating layer on a substrate;
 - forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
 - forming a conductive layer on the insulating layer and the exposed portion of the substrate;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening;

removing the fill layer to a level substantially even with a top of the insulating layer;

removing the conductive layer to a level below the level below the top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer;

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

24. The method of claim 23, wherein the processing proceeds in the order presented.
25. The method of claim 23, wherein removing at least a portion of the insulating layer to expose an outside of the container structure occurs subsequent to forming a dielectric cap on a top of the sidewalls of the conductive layer.
26. The method of claim 23, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:
 - forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and
 - removing the dielectric layer from the insulating layer and the fill layer.
27. The method of claim 26, wherein removing the dielectric layer from the insulating layer and the fill layer further comprises removing the dielectric layer

from the insulating layer and the fill layer using chemical mechanical polishing or blanket etch-back.

28. The method of claim 23, wherein forming an insulating layer on a substrate further comprises forming a layer of borophosphosilicate glass on the substrate.
29. The method of claim 23, wherein forming a conductive layer on the insulating layer and the exposed portion of the substrate further comprises forming a layer of conductively-doped hemispherical grain polysilicon on the insulating layer and the exposed portion of the substrate.
30. The method of claim 23, wherein forming a fill layer on the conductive layer further comprises forming a layer of photoresist on the conductive layer.
31. The method of claim 23, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises forming a cap of silicon oxynitride on a top of the sidewalls of the conductive layer.
32. The method of claim 23, further comprising:
annealing the dielectric cap.
33. A method of forming a semiconductor structure, comprising:
forming an insulating layer on a substrate, wherein the insulating layer comprises at least one insulating material selected from the group consisting of oxides, nitrides and borophosphosilicate glass;
forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate, wherein the conductive layer comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening, further wherein the fill layer comprises a filler material selected from the group consisting of photoresists and high etch-rate oxides;

removing the fill layer to a level substantially even with a top of the insulating layer;

removing the conductive layer to a level below the level below the top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

34. The method of claim 33, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:

forming a layer of the at least one dielectric material on the insulating layer, the conductive layer and the fill layer; and

removing the layer of the at least one dielectric material from the insulating layer and the fill layer.

35. The method of claim 33, further comprising:
annealing the dielectric cap.

36. A container capacitor, comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
a dielectric cap on a top of the sidewalls;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

37. The container capacitor of claim 36, wherein the bottom plate has a cylindrical shape.

38. The container capacitor of claim 36, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

39. The container capacitor of claim 38, wherein the at least one silicon material is conductively doped.

40. The container capacitor of claim 36, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

41. A container capacitor, comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon

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material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

42. The container capacitor of claim 41, wherein the dielectric cap is annealed.

43. A container capacitor, comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

44. The container capacitor of claim 43, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.

45. A container capacitor, comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate is formed by a method comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening; and

removing the conductive layer and the fill layer to a level below a top of the insulating layer;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising:

forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and

removing the dielectric layer from the insulating layer and the fill layer;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

46. The container capacitor of claim 45, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
47. The container capacitor of claim 45, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.
48. The container capacitor of claim 45, wherein the dielectric cap is annealed.

49. A container capacitor, comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate if formed by a method comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening;

removing the fill layer to a level substantially even with a top of the insulating layer; and

removing the conductive layer to a level below the level below the top of the insulating layer;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising:

forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and

removing the dielectric layer from the insulating layer and the fill layer;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

50. The container capacitor of claim 49, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

51. The container capacitor of claim 49, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

52. The container capacitor of claim 49, wherein the dielectric cap is annealed.

53. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
a dielectric cap on a top of the sidewalls;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

54. The semiconductor die of claim 53, wherein the bottom plate has a cylindrical shape.

55. The semiconductor die of claim 53, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

56. The semiconductor die of claim 55, wherein the at least one silicon material is conductively doped.

57. The semiconductor die of claim 53, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

58. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

59. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

60. The semiconductor die of claim 43, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.

61. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate if formed by a method comprising:
forming an insulating layer on the substrate;
forming an opening in the insulating layer,
wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
forming a conductive layer on the insulating layer and the exposed portion of the substrate;
forming a fill layer on the conductive layer,
wherein the fill layer fills the opening; and
removing the conductive layer and the fill layer to a level below a top of the insulating layer;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising:

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forming a dielectric layer on the insulating layer,
the conductive layer and the fill layer; and
removing the dielectric layer from the insulating
layer and the fill layer;

a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is
interposed between the cell plate and the bottom plate.

62. The semiconductor die of claim 61, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

63. The semiconductor die of claim 61, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

64. The semiconductor die of claim 61, wherein the dielectric cap is annealed.

65. A semiconductor die, comprising:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate if formed by a method comprising:
forming an insulating layer on the substrate;
forming an opening in the insulating layer,
wherein the opening has a bottom on an

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exposed portion of the substrate and sidewalls defined by the insulating layer; forming a conductive layer on the insulating layer and the exposed portion of the substrate; forming a fill layer on the conductive layer, wherein the fill layer fills the opening; removing the fill layer to a level substantially even with a top of the insulating layer; and removing the conductive layer to a level below the level below the top of the insulating layer; a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising: forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and removing the dielectric layer from the insulating layer and the fill layer; a dielectric layer on the bottom plate and the dielectric cap; and a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

66. The semiconductor die of claim 65, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
67. The semiconductor die of claim 65, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.
68. The semiconductor die of claim 65, wherein the dielectric cap is annealed.

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69. A memory device, comprising:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
a dielectric cap on a top of the sidewalls;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column access circuit.

70. The memory device of claim 69, wherein the bottom plate has a cylindrical shape.

71. The memory device of claim 69, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

72. The memory device of claim 71, wherein the at least one silicon material is conductively doped.

73. The memory device of claim 69, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

74. A memory device, comprising:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column access circuit.

75. A memory device, comprising:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

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a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is
interposed between the cell plate and the bottom plate;
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column
access circuit.

76. The memory device of claim 75, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.

77. A memory device, comprising:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate if formed by a method comprising:
forming an insulating layer on a substrate;
forming an opening in the insulating layer,
wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
forming a conductive layer on the insulating layer and the exposed portion of the substrate;
forming a fill layer on the conductive layer,
wherein the fill layer fills the opening; and
removing the conductive layer and the fill layer to a level below a top of the insulating layer;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising:

forming a dielectric layer on the insulating layer,
the conductive layer and the fill layer; and
removing the dielectric layer from the insulating
layer and the fill layer;

a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is
interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column
access circuit.

78. The memory device of claim 77, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
79. The memory device of claim 77, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.
80. The memory device of claim 77, wherein the dielectric cap is annealed.
81. A memory device, comprising:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate if formed by a method comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer,

wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate;

forming a fill layer on the conductive layer,

wherein the fill layer fills the opening;

removing the fill layer to a level substantially even with a top of the insulating layer; and

removing the conductive layer to a level below the level below the top of the insulating layer;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap is formed by a method comprising:

forming a dielectric layer on the insulating layer,

the conductive layer and the fill layer; and

removing the dielectric layer from the insulating layer and the fill layer;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

82. The memory device of claim 81, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

83. The memory device of claim 81, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

84. The memory device of claim 81, wherein the dielectric cap is annealed.

85. A memory module, comprising:
a support;
a plurality of leads extending from the support;
a command link coupled to at least one of the plurality of leads;
a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and
at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
a dielectric cap on a top of the sidewalls;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and
the column access circuit.

86. The memory module of claim 85, wherein the bottom plate has a cylindrical shape.
87. The memory module of claim 85, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
88. The memory module of claim 87, wherein the at least one silicon material is conductively doped.
89. The memory module of claim 85, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.
90. A memory module, comprising:
 - a support;
 - a plurality of leads extending from the support;
 - a command link coupled to at least one of the plurality of leads;
 - a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; andat least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

91. A memory module, comprising:

- a support;
- a plurality of leads extending from the support;
- a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

92. The memory module of claim 91, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.
93. A memory system, comprising:
a controller;

a command link coupled to the controller;
a data link coupled to the controller; and
a memory device coupled to the command link and the data link, wherein the memory device comprises:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
a dielectric cap on a top of the sidewalls;
a dielectric layer on the bottom plate and the dielectric cap; and
a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column access circuit.

94. The memory system of claim 93, wherein the bottom plate has a cylindrical shape.
95. The memory system of claim 93, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.
96. The memory system of claim 95, wherein the at least one silicon material is conductively doped.

97. The memory system of claim 93, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

98. A memory system, comprising:

- a controller;
- a command link coupled to the controller;
- a data link coupled to the controller; and
- a memory device coupled to the command link and the data link, wherein the memory device comprises:
 - an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
 - a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
 - a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;
 - a dielectric layer on the bottom plate and the dielectric cap; and
 - a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and
the column access circuit.

99. A memory system, comprising:

- a controller;
- a command link coupled to the controller;
- a data link coupled to the controller; and
- a memory device coupled to the command link and the data link, wherein the memory device comprises:
 - an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
 - a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;
 - a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;
 - a dielectric layer on the bottom plate and the dielectric cap; and
 - a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;
 - a row access circuit coupled to the array of memory cells;
 - a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and
the column access circuit.

100. The memory system of claim 99, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.
101. An electronic system, comprising:
 - a processor; and
 - a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:
 - an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
 - a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;
 - a dielectric cap on a top of the sidewalls;
 - a dielectric layer on the bottom plate and the dielectric cap; and
 - a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.
102. The electronic system of claim 101, wherein the bottom plate has a cylindrical shape.

103. The electronic system of claim 101, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

104. The electronic system of claim 103, wherein the at least one silicon material is conductively doped.

105. The electronic system of claim 101, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

106. An electronic system, comprising:
a processor; and
a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:
an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one

dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

107. An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

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a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

108. The electronic system of claim 107, wherein the dielectric cap is annealed at approximately 600°C to 1000°C for approximately 10 to 20 seconds.
109. A method of forming a semiconductor structure, comprising:
forming a conductive container structure having a closed bottom and sidewalls
extending upward from the closed bottom; and
forming a dielectric cap on a top of the sidewalls.
110. The method of claim 109, wherein the processing proceeds in the order presented.
111. The method of claim 109, wherein forming a dielectric cap on a top of the sidewalls further comprises forming a dielectric cap of silicon oxynitride on a top of the sidewalls.
112. The method of claim 109, further comprising:
annealing the dielectric cap.
113. A method of forming a semiconductor structure, comprising:
forming a conductive container structure having a closed bottom and sidewalls
extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon; and

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forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

114. The method of claim 113, wherein the processing proceeds in the order presented.

115. A method of forming a semiconductor structure, comprising:
forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides; and
annealing the dielectric cap.

116. The method of claim 115, wherein the processing proceeds in the order presented.

117. A method of forming a container capacitor, comprising:
forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom;
forming a dielectric cap on a top of the sidewalls;
forming a dielectric layer on the conductive container structure and the dielectric cap; and
forming a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the conductive container structure.

118. The method of claim 117, wherein the processing proceeds in the order presented.

119. The method of claim 117, wherein forming a dielectric cap on a top of the sidewalls further comprises forming a dielectric cap of silicon oxynitride on a top of the sidewalls.

120. The method of claim 117, further comprising:
annealing the dielectric cap.

121. A method of forming a container capacitor, comprising:
forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;
forming a dielectric layer on the conductive container structure and the dielectric cap; and
forming a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the conductive container structure.

122. The method of claim 121, wherein the processing proceeds in the order presented.

123. A method of forming a container capacitor, comprising:

forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

annealing the dielectric cap;

forming a dielectric layer on the conductive container structure and the dielectric cap; and

forming a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the conductive container structure.

124. The method of claim 123, wherein the processing proceeds in the order presented.